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National Semiconductor

→26163

May 1983

MM5437 Digital Noise Source

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General Description

The MM5437 device is a monolithic metal gate NMOS integrated circuit which may be used as a digital noise source or a pseudo-random number generator. The part is designed to produce a broadband white noise signal with uniform noise quality and output amplitude. Two outputs are provided. The first, OUT 1, is sequence-limited to reduce "thumps." The other output, OUT 2, is the last stage of the shift register when $\overline{\text{CONTROL 2}}$ is left floating or is pulled up. Typical cycle time is one minute. Data is clocked in and out on the rising edge of the clock.

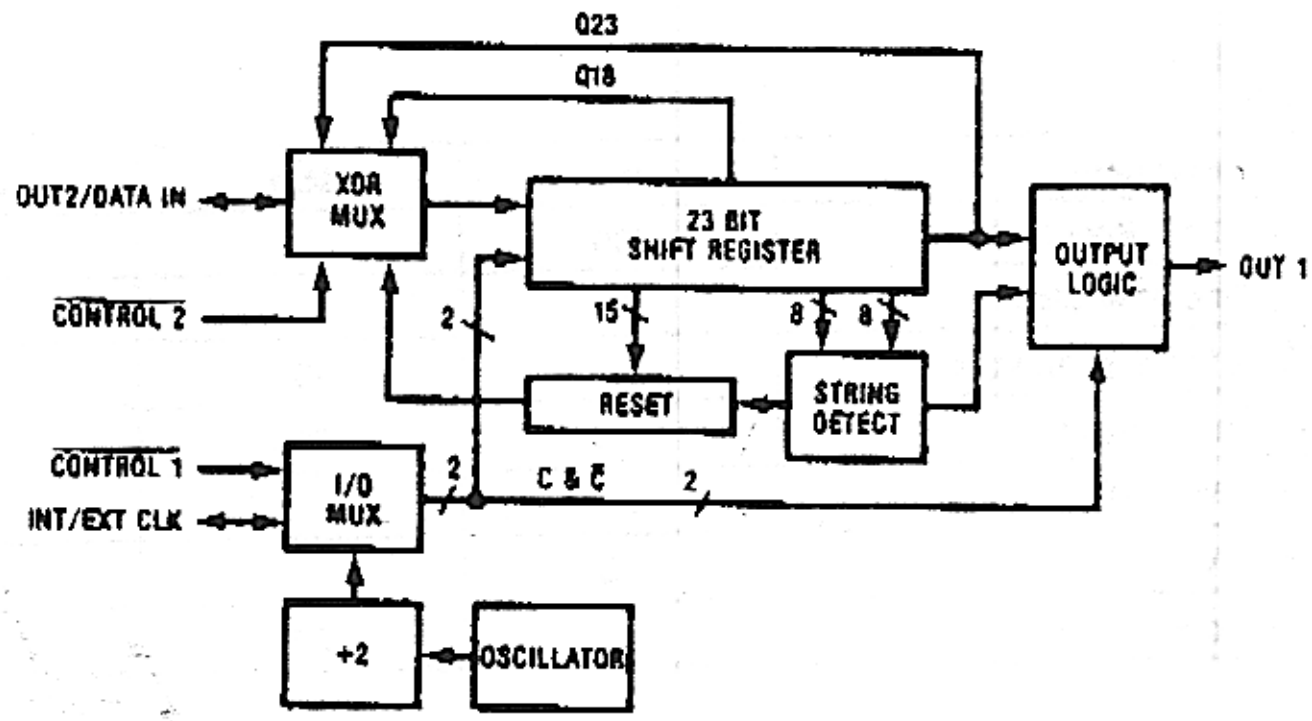
Applications

- Electronic musical rhythm instrument sound generators
- Music synthesizer white and pink noise generators
- Room acoustics testing/equalization
- ~~Pseudo-random number generator~~

Features

- Internal self-contained oscillator
- Single supply voltage range of 4.5V to 11V
- TTL compatible at 5V
- Normal and sequence-limited outputs
- Low power consumption
- One minute cycle time
- External loading and clocking capability
- Automatic reset for all-zeros state
- Uniform noise quality
- Uniform noise amplitude
- Eliminate noise preamps
- Single component insertion

Block and Connection Diagrams



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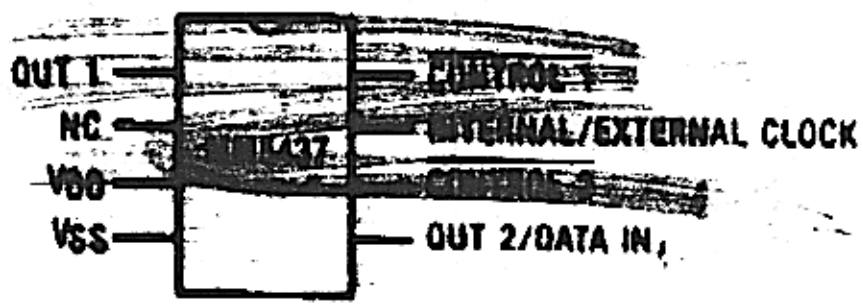

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Top View

Absolute Maximum Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Operating Supply Voltage, V_{DD}	12V
Storage Temperature, T_S	−65°C to +150°C
Operating Temperature, T_A	−40°C to +85°C
DC Output Current, per pin	±12 mA
Lead Temperature (Soldering; 10s)	+300°C

DC Electrical Characteristics T_A within operating range, V_{SS} = 0V, V_{DD} = 11V, unless specified

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage (V_{DD})		4.5		11	V
Supply Current (I_{DD})	V_{DD} = 4.5V (No load) V_{DD} = 11V (No load)			4 5	mA mA
Output Voltage Levels Logic '0' Logic '1'	 I_{OL} = +1.6 mA, V_{DD} = 4.5V I_{OH} = −400 µA, V_{DD} = 4.5V	 V_{SS} 2.4		 0.4 V_{DD}	 V V
Input Voltage Levels Logic '0' Logic '1'		 2.0		 0.8	 V
Input Currents Logic '0' Logic '1'	 V_{IN} = 0.4V V_{IN} = 2.4V			 200 200	 µA µA
Half Power Point*		30		140	kHz
Cycle Time		25		110	sec.

*Half Power Point = 0.45 (Shift Register Clock Frequency)

AC Timing $-40°C \le T_A \le +85°C$, $4.5V \le V_{DD} \le 11V$

Symbol	Parameter	Min	Max	Units
t_S	Data Set Up Time Prior to Clock	100		ns
t_H	Data Hold Time After Clock	100		ns
t_{C2DV}	$\overline{\text{CONTROL 2}}$ to Data Out Valid		100	ns
t_{CLKDV}	Clock to Data Out Valid		700	ns
t_{PH}	Clock Pulse Width High	1.5		µs
t_{PL}	Clock Pulse Width Low	1.5		µs
t_r, t_f	Input Rise and Fall Times		220	ns

Inputs/Outputs

$\overline{\text{CONTROL 1}}$: A mode switch input, which when held at a logic "1" or left floating, gates the internal oscillator onto the INT/EXT CLK pin. When $\overline{\text{CONTROL 1}}$ is at a logic "0", the shift register can be driven externally through the INT/EXT CLK pin.

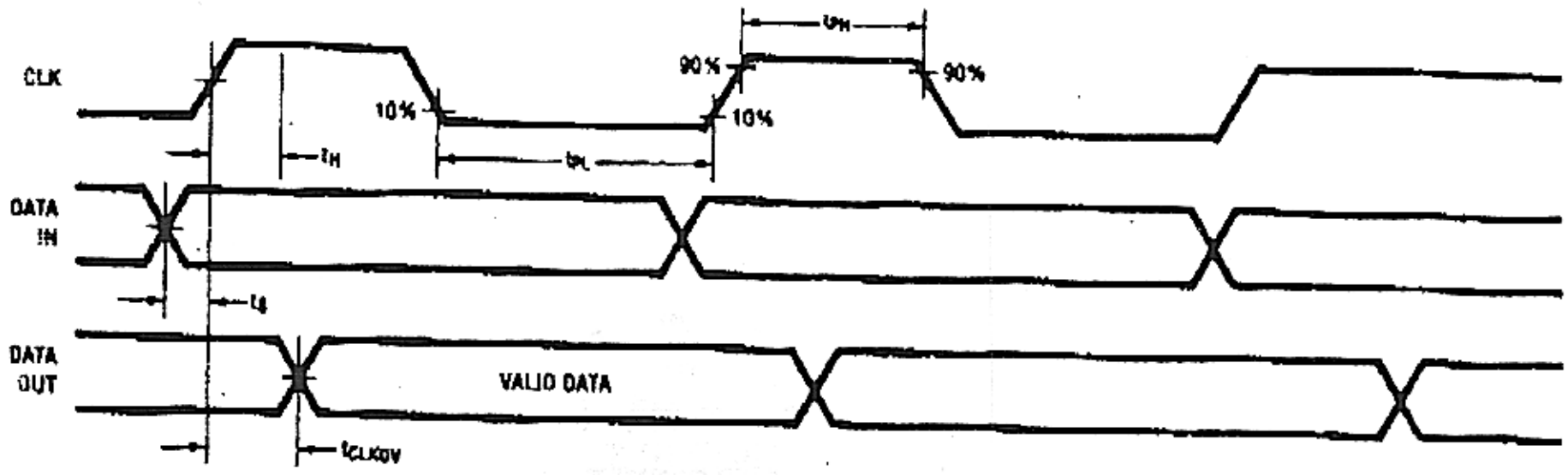
$\overline{\text{CONTROL 2}}$: A mode switch input, which when held at a logic "1" or left floating, gates the last stage of the shift register onto the OUT 2/DATA IN pin. When $\overline{\text{CONTROL 2}}$ is at a logic "0", the shift register can be loaded externally through the OUT 2/DATA IN pin.

OUT 1: An output pin for the sequence-limited output from the shift register.

INT/EXT CLK: An input/output pin. See $\overline{\text{CONTROL 1}}$ for description.

OUT 2/DATA IN: An input/output pin. See $\overline{\text{CONTROL 2}}$ for description.

Timing Diagrams



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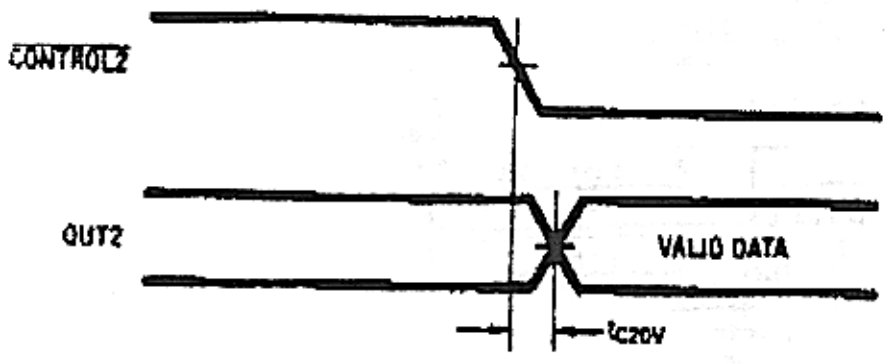

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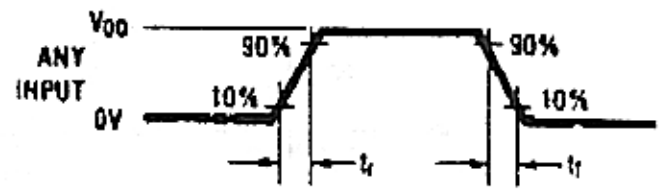

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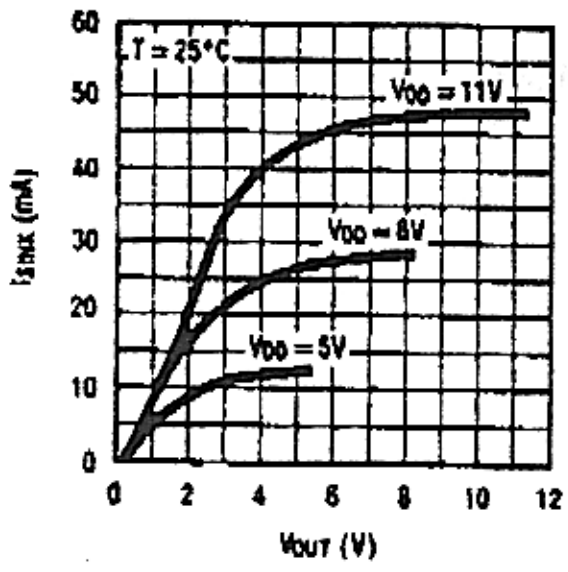

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FIGURE 1. I_{SINK} vs V_{OUT}

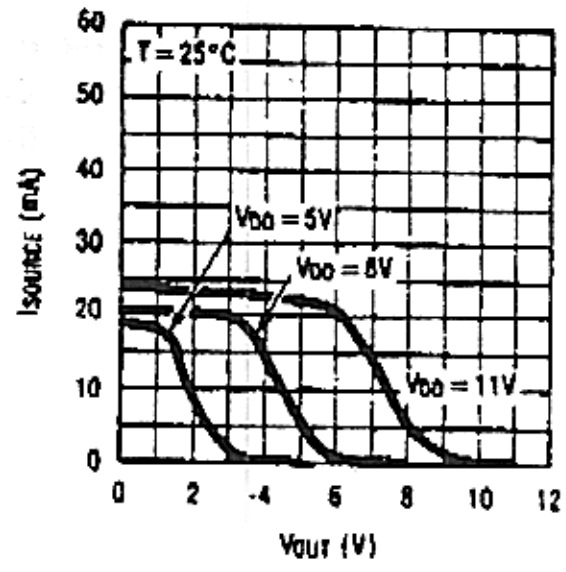

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FIGURE 2. I_{SOURCE} vs V_{OUT}

Typical Applications

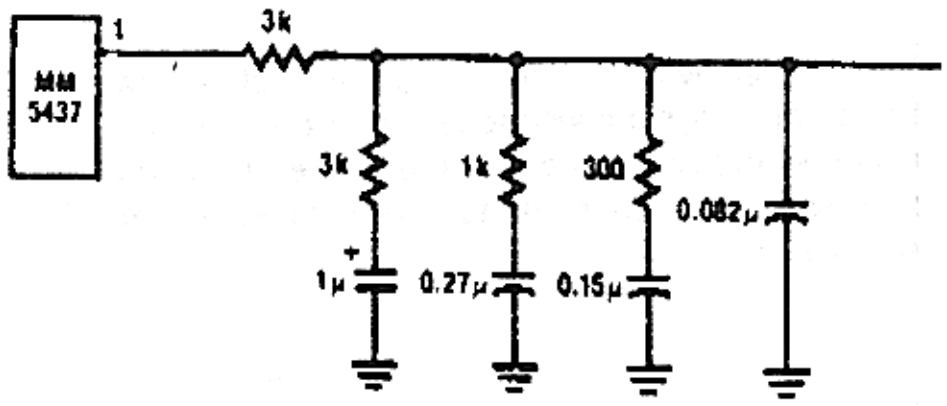

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FIGURE 3. Pink Noise Generator

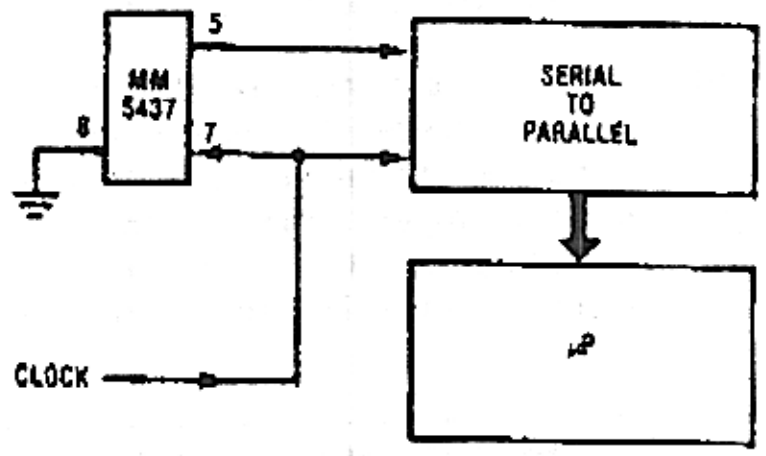

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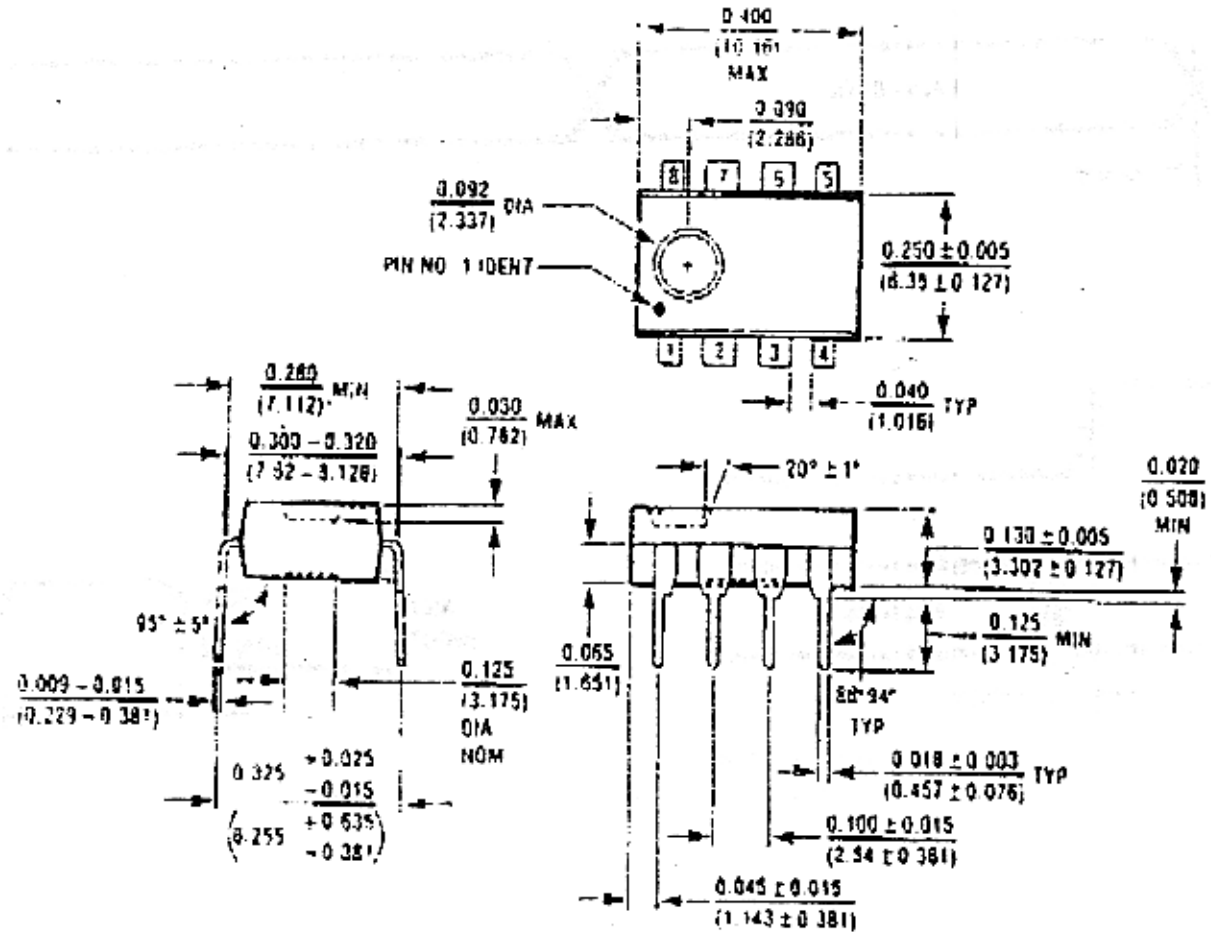
FIGURE 4. Pseudo-Random Number Generator

Physical Dimensions inches (millimeters)



8-Lead Molded Dual-In-Line Package (N)
Order Number MM5437N
NS Package Number N08E

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